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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,764	12/29/2000	Sailesh Kottapalli	2207/10122	3475

7590 03/19/2004

Kenyon & Kenyon
Suite 600
333 W. San Carlos Street
San Jose, CA 95110-2711

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/753,764	Applicant(s) KOTTAPALLI, SAILESH
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #3. Declaration/Fee as received on 4/9/2001 and #4. Drawings as received on 4/9/2001.

Specification

3. The disclosure is objected to because of the following informalities: On page 5, line 2, it is recommended that applicant replace the phrase "components 122,124,126,128,130 have been labeled 1-5" with --components 122,124,126,128,130,132 have been labeled 1-6.

Appropriate correction is required.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Fig.2, the examiner has been unable to find reference numbers 202, 206, 208, 210, 212, 214, 216, 234, 236, 238, 240, 242, and 244 within the specification. In Fig.3, the examiner has been unable to find reference numbers 302, 308, 310, 312, 314, 316, 334, 336, 338, 340, 342, and 344 within the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the

reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "212" has been used to designate both the EXE stage and re-steer logic component 1. The examiner recommends changing the reference number assigned to re-steer logic component 1 from 212 to 222 to match page 7, lines 16 and 20 of the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to because of the following minor informalities: Regarding Fig.2 and Fig.3, the examiner asserts that it is difficult to determine from which wires the MUX inputs are coming from. For instance, looking at Fig.2, it is difficult to determine whether the 4th and 6th MUX2 inputs from the bottom originate from the curved wire or the straight wire. Similar problems occur in Fig.3. The examiner recommends either adding more lateral space between the wires, eliminating the "hop-overs" (which indicate crossing wires which are not connected) or an improvement left to applicant's discretion. Consequently, if and when this application is allowed, the figure will be viewed much more clearly by the public. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claim 1 is objected to because of the following informalities: In lines 2 and 3, replace "associated to" with --associated with--. Also, in lines 2 and 3, it is not clear to the examiner what a first/second thread of instruction pointers is. The examiner recommends rewording this to something along the lines of "instruction pointers of a first/second thread". Appropriate correction is required.

8. Claim 10 is objected to because of the following informalities: In lines 2 and 3, replace "multiplexer to" with --multiplexer with--. Also, in lines 2 and 3, it is not clear to the examiner what a first/second thread of instruction pointers is. The examiner recommends rewording this to something along the lines of "instruction pointers of a first/second thread". Appropriate correction is required.

9. Claim 19 is objected to because of the following informalities: In lines 2 and 3, replace "associated to" with --associated with--. Also, in lines 2 and 3, it is not clear to the examiner what a first/second thread of instruction pointers is. The examiner recommends rewording this to something along the lines of "instruction pointers of a first/second thread". Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the

invention. In line 4, a reference is made to "instruction pointers". It is not clear whether applicant is introducing a new set of instruction pointers or if these pointers are the pointers belonging to the first and second threads. In line 10, a reference is made to "instruction pointers". It is not clear whether applicant is introducing a new set of instruction pointers or if these pointers are the same as those provided by the multiplexers. In line 11, a reference is made to "the instruction pointers". It is not clear whether these pointers are the same as those provided by the multiplexers (from line 4) or the pointers associated with one of the threads (from lines 2-3). Finally, in line 11, a "storage element" is referenced. It is not clear whether this storage element is a newly introduced storage element or whether it is one of the first and second storage elements couples to the first and second multiplexers.

12. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 4, a reference is made to "instruction pointers". It is not clear whether applicant is introducing a new set of instruction pointers or if these pointers are the pointers belonging to the first and second threads. In lines 10 and 11, references are made to "the instruction pointers". It is not clear whether these pointers are the same as those provided by the multiplexers (from line 4) or the pointers associated with one of the threads (from lines 2-3). Finally, in line 11, a "storage element" is referenced. It is not clear whether this storage element is a newly introduced storage element or whether it is one of the first and second storage elements couples to the first and second multiplexers.

13. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. In line 4, a reference is made to "instruction pointers". It is not clear whether applicant is introducing a new set of instruction pointers or if these pointers are the pointers belonging to the first and second threads. In line 10, a reference is made to "instruction pointers". It is not clear whether applicant is introducing a new set of instruction pointers or if these pointers are the same as those provided by the multiplexers. In line 11, a reference is made to "the instruction pointers". It is not clear whether these pointers are the same as those provided by the multiplexers (from line 4) or the pointers associated with one of the threads (from lines 2-3). Finally, in line 11, a "storage element" is referenced. It is not clear whether this storage element is a newly introduced storage element or whether it is one of the first and second storage elements couples to the first and second multiplexers.

14. The examiner's interpretation of each of claims 1, 10, and 19, will be evident in the rejections below.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

16. Claims 1-4, 9-13, and 18-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (herein referred to as AAPA).

17. Referring to claim 1, AAPA has taught a simultaneous multithreaded processor system comprising:

a) a first multiplexer associated to a first thread of instruction pointers. See Fig.2, component 218.

b) a second multiplexer associated to a second thread of instruction pointers. See Fig.2, component 220.

c) said first and second multiplexers to provide instruction pointers for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

d) first and second storage elements coupled to said respective first and second multiplexers (see Fig.2, components 248 and 250, for instance, and note that they are coupled to MUXs 218 and 220), wherein:

d1) one of the first and second threads is active while the other of said first and second threads is inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

d2) and instruction pointers for the active thread are delivered to processor logic and the instruction pointers for the inactive thread are delivered to a storage element for delivery to the processor logic when the inactive thread becomes the active thread. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. For an inactive thread (second thread), the instruction pointers are delivered by re-steer logic 230 and 232, for instance, to storage elements 248 and 250. The storage elements are then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor

logic when the second thread becomes active. It should be noted that based on the 112 rejection above, the examiner is able to interpret "the instruction pointers for the inactive thread" as being instruction pointers belonging to an inactive thread, as described in lines 2-3 of claim 1. The instruction pointers do not necessarily have to be the same instruction pointers that are outputted by multiplexers 218 and 220.

18. Referring to claim 2, AAPA has taught a system as described in claim 1. AAPA has further taught a common multiplexer coupled between said first and second multiplexer and processor logic. See Fig.2, component 246.

19. Referring to claim 3, AAPA has taught a system as described in claim 2. AAPA has further taught that the common multiplexer receives instruction pointer data sequentially from the first multiplexer and the second multiplexer by utilizing a time-multiplexing protocol. See page 2, lines 17-19, of applicant's specification (background information section).

20. Referring to claim 4, AAPA has taught a system as described in claim 3. AAPA has further taught that the time-multiplexing protocol is a `round-robin` protocol. See page 2, lines 17-19, of applicant's specification (background information section).

21. Referring to claim 9, AAPA has taught a system as described in claim 1. AAPA has further taught that the storage element is a flip-flop device. See page 2, line 21.

22. Referring to claim 10, AAPA has taught a method for a simultaneous multithreaded processor system, comprising the steps of:

a) associating a first multiplexer to a first thread of instruction pointers. See Fig.2, component 218.

b) associating a second multiplexer to a second thread of instruction pointers. See Fig.2, component 220.

c) providing, by said first and second multiplexers, instruction pointers for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

d) coupling first and second storage elements to said respective first and second multiplexers. see Fig.2, components 248 and 250, for instance, and note that they are coupled to MUXs 218 and 220

e) establishing one of the first and second threads as active and the other of said first and second threads as inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

f) delivering the instruction pointers for the active thread to processor logic; and delivering the instruction pointers for the inactive thread to a storage element for delivery to the processor logic when the inactive thread becomes the active thread. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. For an inactive thread (second thread), the instruction pointers are delivered by re-steer logic 230 and 232, for instance, to storage elements 248 and 250. The storage elements are then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the second thread becomes active.

23. Referring to claim 11, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 2 performs the method of claim 11. Therefore, claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

24. Referring to claim 12, AAPA has taught a method as described in claim 11. Furthermore, the system of claim 3 performs the method of claim 12. Therefore, claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

25. Referring to claim 13, AAPA has taught a method as described in claim 12. Furthermore, the system of claim 4 performs the method of claim 13. Therefore, claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

26. Referring to claim 18, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 9 performs the method of claim 18. Therefore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

27. Referring to claim 19, AAPA has taught a simultaneous multithreaded processor system comprising:

a) a first multiplexer associated to a first thread of instruction pointers. See Fig.2, component 218.

b) a second multiplexer associated to a second thread of instruction pointers. See Fig.2, component 220.

c) said first and second multiplexers to provide instruction pointers for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

d) first and second storage elements coupled to said respective first and second multiplexers (see Fig.2, components 248 and 250, for instance, and note that they are coupled to MUXs 218 and 220), wherein:

d1) one of the first and second threads is active while the other of said first and second threads is inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

d2) instruction pointers for the active thread are delivered to processor logic and the instruction pointers for the inactive thread are delivered to a storage element for delivery to the processor logic when the inactive thread becomes the active thread. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. For an inactive thread (second thread), the instruction pointers are delivered by re-steer logic 230 and 232, for instance, to storage elements 248 and 250. The storage elements are then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the second thread becomes active.

d3) and a common multiplexer coupled between said first and second multiplexer and processor logic that receives instruction pointer data sequentially from the first multiplexer and the second multiplexer by utilizing a time-multiplexing protocol. See Fig.2, component 246, and see page 2, lines 17-19, of applicant's specification (background information section).

28. Referring to claim 20, AAPA has taught a system as described in claim 19. AAPA has further taught that the first multiplexer and the second multiplexer receive instruction pointer information and data from a plurality of stages in a processor pipeline. See Fig.2, and note that MUXs 218 and 220 receive pointer information and data from various pipeline stages, including the IPG-1, IPG+1, IPG+2, and CMT stages.

29. Referring to claim 21, AAPA has taught a system as described in claim 20. AAPA has further taught that the first multiplexer and the second multiplexer receive instruction pointer information and data from re-steer logic at the plurality of stages in the processor pipeline. See Fig.2, and note that the information is received from re-steer logic located in a plurality of pipeline stages (the re-steer logic includes the boxes labeled 1-6).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 5-8, 14-17, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, as applied above.

32. Referring to claim 5, AAPA has taught a system as described in claim 1. Although AAPA's Fig.2 utilizes time-multiplexing between two threads (page 2, lines 17-19), AAPA has not explicitly taught that the first multiplexer and the second multiplexer are priority multiplexers. However, AAPA also shows that priority multiplexers are known in the art. See

Fig.1. In addition, from page 2, lines 6-9 of applicant's specification, it has been taught that a thread may be switched if a higher priority thread needs attention. As a result, it would have been obvious to one of ordinary skill in the art to modify the first and second multiplexers of Fig.2 to be priority multiplexers so that more important threads, having highest priority, are executed as soon as possible.

33. Referring to claim 6, AAPA has taught a system as described in claim 5. AAPA has further taught that the first multiplexer and the second multiplexer receive instruction pointer information and data from a plurality of stages in a processor pipeline. See Fig.2, and note that MUXs 218 and 220 receive pointer information and data from various pipeline stages, including the IPG-1, IPG+1, IPG+2, and CMT stages.

34. Referring to claim 7, AAPA has taught a system as described in claim 6. AAPA has further taught that the first multiplexer and the second multiplexer receive instruction pointer information and data from re-steer logic at the plurality of stages in the processor pipeline. See Fig.2, and note that the information is received from re-steer logic located in a plurality of pipeline stages (the re-steer logic includes the boxes labeled 1-6).

35. Referring to claim 8, AAPA has taught a system as described in claim 7. AAPA has not explicitly taught that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority. However, AAPA has taught the concept of a multiplexer which passes instruction pointer information and data with a pre-determined priority. See Fig.1, and page 4, line 16, to page 5, line 9, of applicant's specification. Such a multiplexer allows for switching threads such that the highest priority thread receives immediate attention. See page 2, lines 6-9 of applicant's specification.

As a result, it would have been obvious to one of ordinary skill in the art to modify Fig.2 of AAPA such that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority so that more important threads, having highest priority, are executed as soon as possible.

36. Referring to claim 14, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 5 performs the method of claim 14. Therefore, claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

37. Referring to claim 15, AAPA has taught a method as described in claim 14. Furthermore, the system of claim 6 performs the method of claim 15. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

38. Referring to claim 16, AAPA has taught a method as described in claim 15. Furthermore, the system of claim 7 performs the method of claim 16. Therefore, claim 16 is rejected for the same reasons set forth in the rejection of claim 7 above.

39. Referring to claim 17, AAPA has taught a method as described in claim 16. Furthermore, the system of claim 8 performs the method of claim 17. Therefore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

40. Referring to claim 22, AAPA has taught a system as described in claim 19. AAPA has not explicitly taught that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority. However, AAPA has taught the concept of a multiplexer which passes instruction pointer information and data with a pre-determined priority. See Fig.1, and page 4, line 16, to page 5, line 9, of applicant's specification. Such a multiplexer allows for switching threads such that the highest

priority thread receives immediate attention. See page 2, lines 6-9 of applicant's specification. As a result, it would have been obvious to one of ordinary skill in the art to modify Fig.2 of AAPA such that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority so that more important threads, having highest priority, are executed as soon as possible.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Parady, U.S. Patent No. 5,933,627, has taught a thread switching system in which instruction pointers for inactive threads are stored in separate storage elements. These instruction pointers specify resume points within the inactive threads once they become active.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 17, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100